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(54) SHIFT REGISTER UNIT, SHIFT REGISTER CIRCUIT, ARRAY SUBSTRATE AND DISPLAY DEVICE

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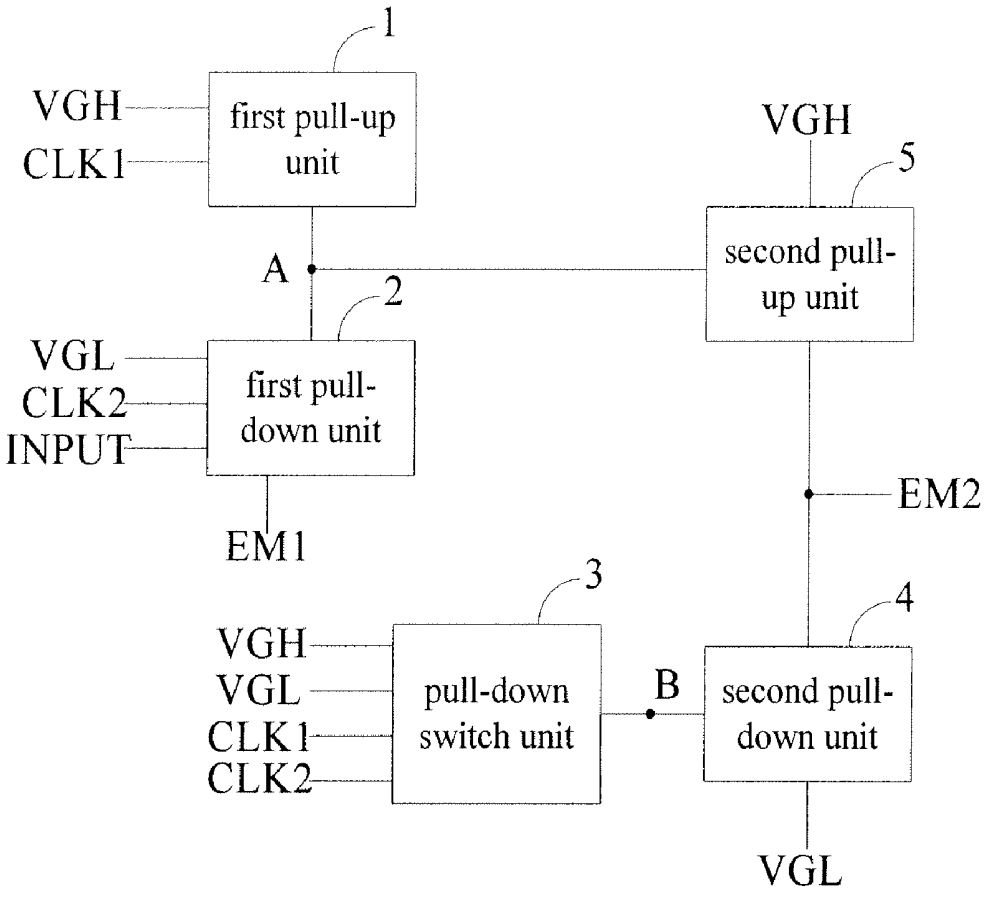
(57) **ABSTRACT**

A shift register unit, a shift register circuit, an array substrate and a display device are provided. The present disclosure relates to the field of display device manufacture, and can prevent an OLED device from flickering while writing display data. A shift register comprises a first pull-up unit, connected with a high level end, a first clock signal end and a first control node (A); a first pull-down unit, connected with a low level end, a second clock signal end, an input signal end, the first pull-up unit, a first output end and the first control node (A); a pull-down switch unit, connected with the high level end, the low level end, the first clock signal end, the second clock signal end and a second control node (B); a second pull-down unit, connected with the low level end, the second control node (B) and a second output end; and a second pull-up unit, connected with the high level end, the first control node (A) and the second output end.



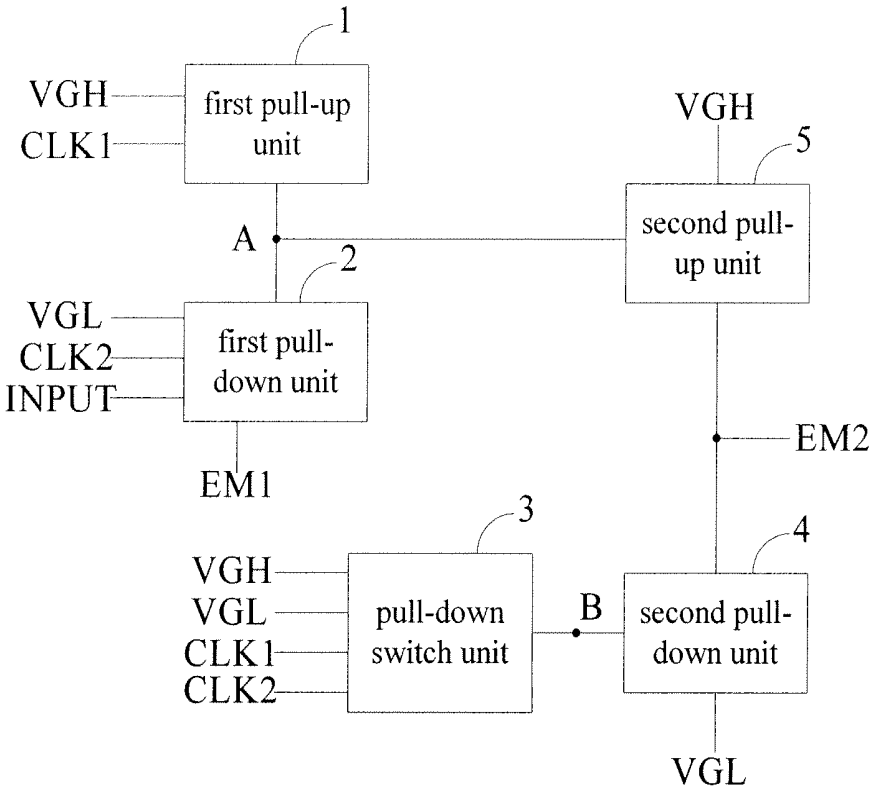

1
VGH
CLK1
first pull-up unit
VGH
5
second pull-up unit
A
2
VGL
CLK2
INPUT
first pull-down unit
EM2
EM1
3
4
VGH
VGL
CLK1
CLK2
pull-down switch unit
B
second pull-down unit
VGL

Figure 1

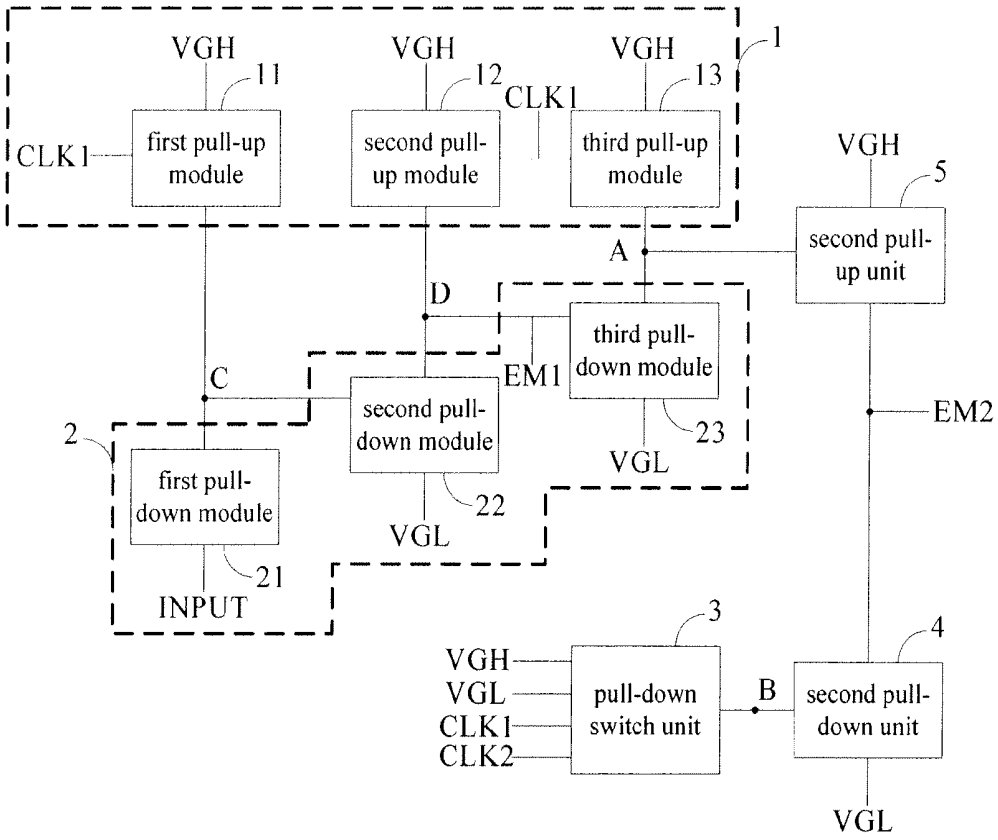

VGH
VGH
VGH
1
11
12
13
CLK1
CLK1
first pull-up module
second pull-up module
third pull-up module
VGH
5
second pull-up unit
A
D
third pull-down module
EM1
C
second pull-down module
EM2
2
23
VGL
first pull-down module
22
VGL
21
INPUT
3
4
VGH
VGL
CLK1
CLK2
pull-down switch unit
B
second pull-down unit
VGL

Figure 2

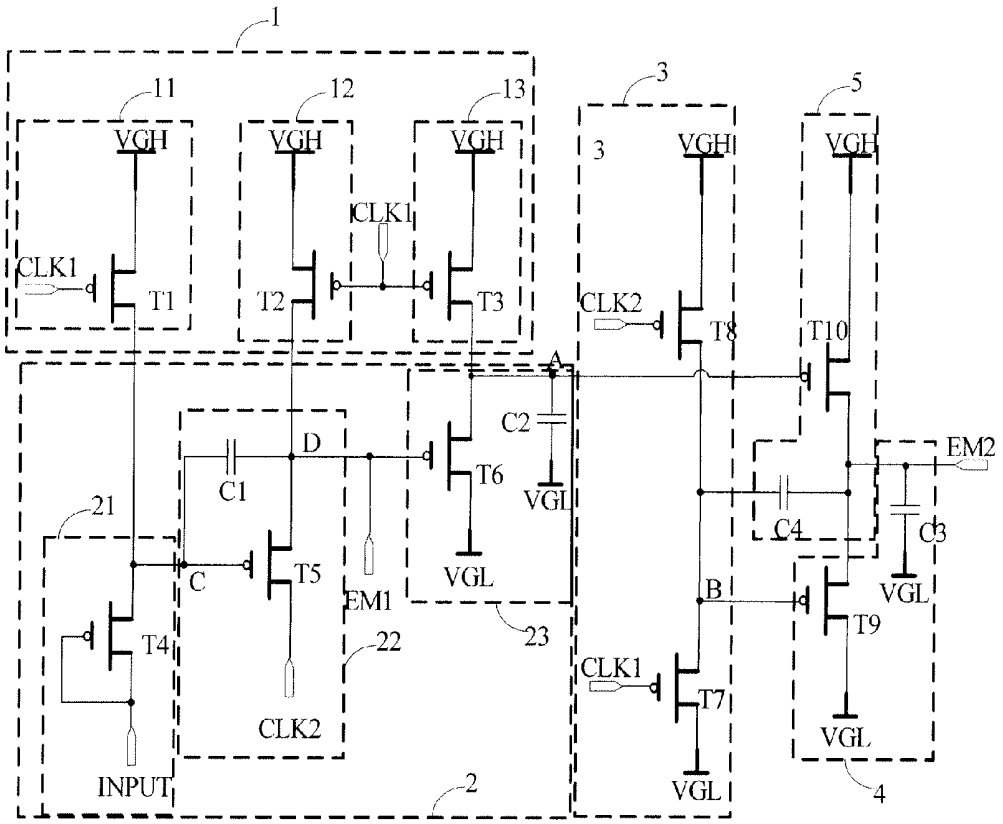

1
11
12
13
3
5
VGH
VGH
VGH
3
VGH
VGH
CLK1
CLK1
CLK1
T1
T2
T3
CLK2
T8
T10
A
C2
D
C1
T6
VGL
EM2
21
C4
C3
C
T5
EM1
VGL
VGL
B
T4
22
23
T9
CLK1
T7
CLK2
VGL
VGL
INPUT
2
4

Figure 3

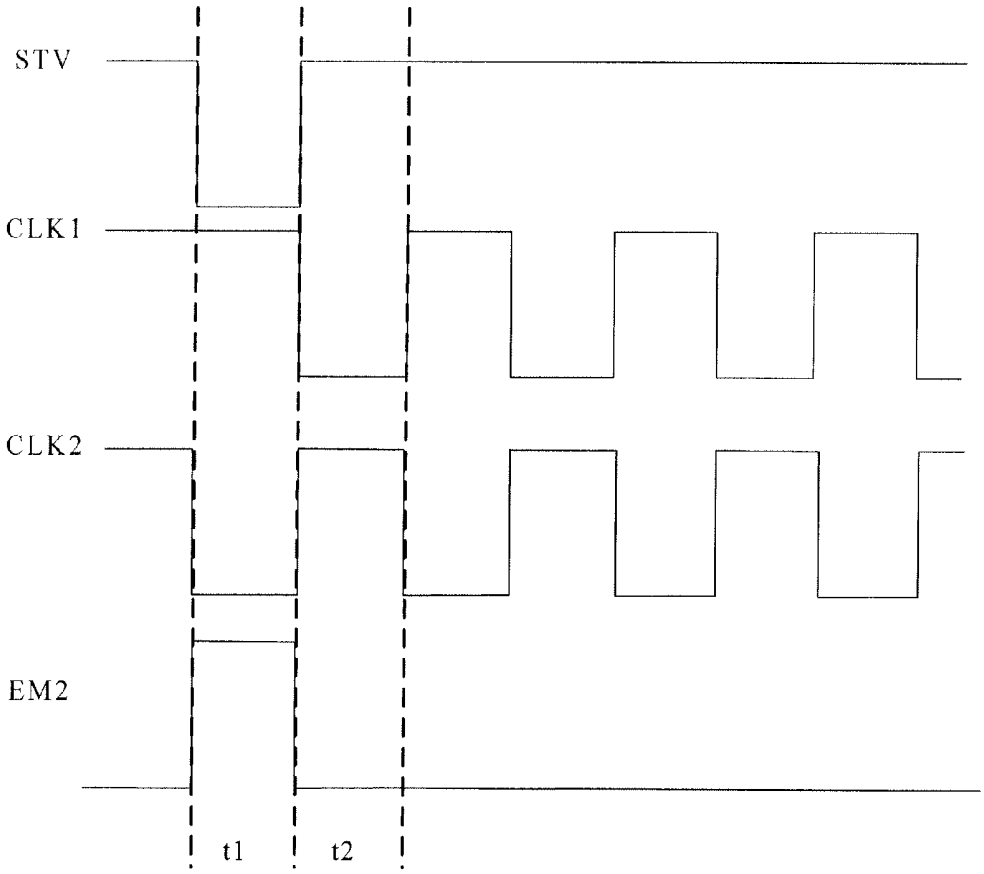


Figure 4

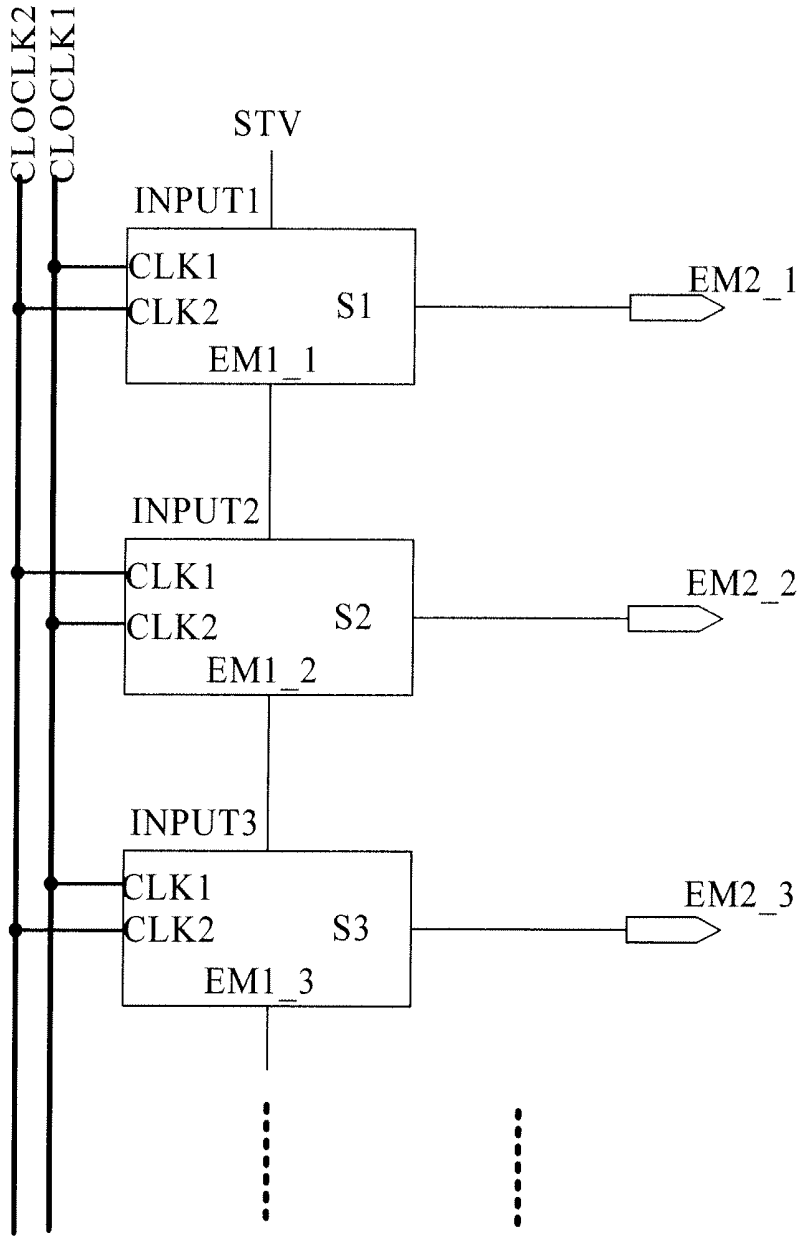

CLOCLK2
CLOCLK1
STV
INPUT1
CLK1
CLK2
S1
EM1_1
EM2_1
INPUT2
CLK1
CLK2
S2
EM1_2
EM2_2
INPUT3
CLK1
CLK2
S3
EM1_3
EM2_3

Figure 5

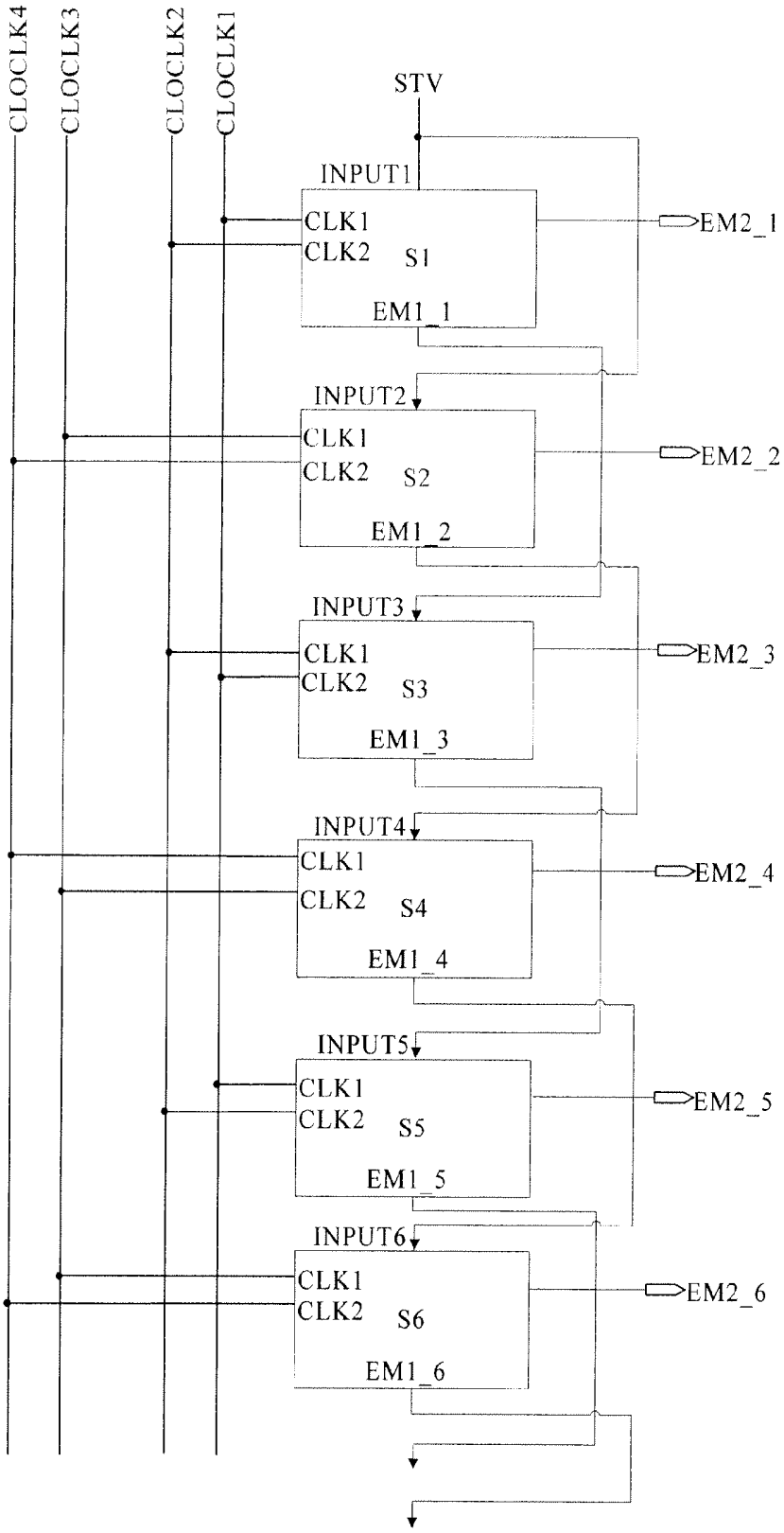

CLOCLK4
CLOCLK3
CLOCLK2
CLOCLK1
STV
INPUT1
CLK1
CLK2
S1
EM1_1
EM2_1
INPUT2
CLK1
CLK2
S2
EM1_2
EM2_2
INPUT3
CLK1
CLK2
S3
EM1_3
EM2_3
INPUT4
CLK1
CLK2
S4
EM1_4
EM2_4
INPUT5
CLK1
CLK2
S5
EM1_5
EM2_5
INPUT6
CLK1
CLK2
S6
EM1_6
EM2_6

Figure 6

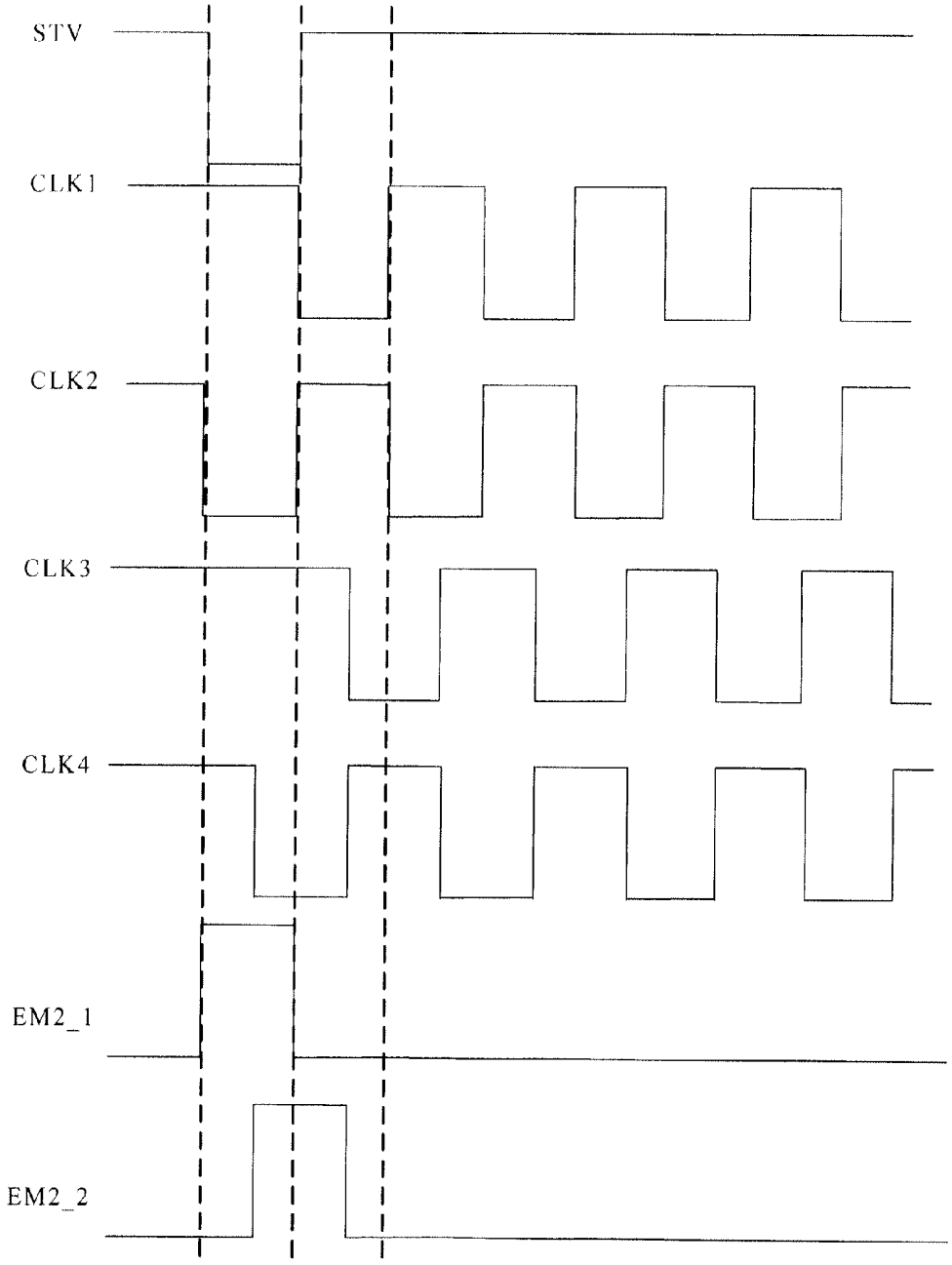


Figure 7

SHIFT REGISTER UNIT, SHIFT REGISTER CIRCUIT, ARRAY SUBSTRATE AND DISPLAY DEVICE

TECHNICAL FIELD

[0001] The present disclosure relates to the field of display device manufacture, particularly to a shift register unit, a shift register circuit, an array substrate and a display device.

BACKGROUND

[0002] With the continuous development of display technology, development of a display in recent years gradually shows a development trend of high integration and low cost. A kind of very important technology therein is implementation of mass production of GOA (Gate Driver on Array) technology. By using the GOA technology, a TFT (Thin Film Transistor) gate switch circuit is integrated on an array substrates of a display panel to form a scanning driver for the display panel, thereby capable of omitting the IC part for a gate driver. This can not only lower product cost in both of material cost and manufacturing process, but also enable the display panel to have a beautiful design of two symmetrical sides and a narrow border. In the meantime, since a process for bonding in the direction of the Gate can be omitted, it is useful for increasing productivity and a yield rate. This kind of gate switch circuit being integrated on an array substrate by using the GOA technology is also referred to as a GOA circuit or a shift register circuit.

[0003] Since the GOA circuit has the above mentioned advantages, the current OLED (Organic Light-Emitting Diode) display has increasingly used the GOA circuit as a row gating control signal of the gate of a pixel circuit array TFT. For the OLED display, since an OLED is a current driving device, the light emission of the OLED device can be controlled by controlling a current channel into the OLED device. In order to perform accurate control on the driving current of the OLED device, a driving TFT is usually added on the basis of a pixel circuit to perform accurate control on the driving current of the OLED device.

[0004] The disadvantage of this kind of circuit consists in that when a driving current is inputted to the OLED device at the moment when the GOA circuit drives a pixel circuit, which results in that there occurs a flicker in the OLED display device while writing display data, thus affecting the quality of the product.

SUMMARY

[0005] The embodiments of the present disclosure provide a shift register unit, a shift register circuit, an array substrate and a display device, which can prevent the OLED display device from flickering while writing display data.

[0006] In order to achieve the above object, the embodiments of the present disclosure adopt the following technical solutions.

[0007] According to an aspect of the embodiments of the present disclosure, there is provided a shift register unit comprising:

a first pull-up unit connected with a high level end, a first clock signal end and a first control node A;

a first pull-down unit connected with a low level end, a second clock signal end, an input signal end, the first pull-up unit, a first output end and the first control node A;

a pull-down switch unit connected with the high level end, the low level end, the first clock signal end, the second clock signal end and a second control node B;

a second pull-down unit connected with the low level end, the second control node B and a second output end; and

a second pull-up unit connected with the high level end, the first control node A and the second output end;

wherein, the first pull-up unit is used to pull up a level of the first control node A when a low level is inputted into the first clock signal end; the first pull-down unit is used to pull down the level of the first control node A when a low level is inputted into both of the second clock signal end and the input signal end, respectively; the pull-down switch unit is used to pull down a level of the second control node B when a low level is inputted into the first clock signal end, and pull up the level of the second control node B when a low level is inputted into the second clock signal end; the second pull-up unit is used to pull up a level outputted from the second output end when the first control node A is at a low level, to output a driving signal; and the second pull-down unit is used to pull down the level outputted from the second output end when the second control node B is at a low level, to reset the driving signal.

[0008] The first pull-up unit comprises:

a first pull-up module connected with the high level end, the first clock signal end and a third control node C;

a second pull-up module connected with the high level end, the first clock signal end and a fourth control node D; and

a third pull-up module connected with the high level end, the first clock signal end and the first control node A,

correspondingly, the first pull-down unit comprises:

a first pull-down module connected with the input signal end and the third control node C;

a second pull-down module connected with the second clock signal end, the third control node C and the fourth control node D; and

a third pull-down module connected with the low level end, the fourth control node D and the first control node A,

wherein the first output end is connected with the fourth control node D.

[0009] The first pull-up module comprises a first transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the third control node C.

[0010] the second pull-up module comprises a second transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the fourth control node D.

[0011] the third pull-up module comprises a third transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the first control node A.

[0012] the first pull-down module comprises a fourth transistor having a gate and source connected with the input signal end, and having a drain connected with the third control node C.

[0013] the second pull-down module comprises a fifth transistor and a first capacitor, a gate of the fifth transistor is connected with the third control node C, a source of the fifth transistor is connected with the second clock signal end, a drain of the fifth transistor is connected with the fourth control node D, and two ends of the first capacitor are connected with the gate and the source of the fifth transistor, respectively.

[0014] the third pull-down module comprises a sixth transistor and a second capacitor, a gate of the sixth transistor is connected with the fourth control node D, a source of the sixth transistor is connected with the low level end, a drain of the sixth transistor is connected with the first control node A, and two ends of the second capacitor are connected with the source and the drain of the sixth transistor, respectively.

[0015] the pull-down switch unit comprises a seventh transistor and an eighth transistor, a gate of the seventh transistor is connected with the first clock signal end, a source of the seventh transistor is connected with the low level end, a drain of the seventh transistor is connected with the second control node B, a gate of the eighth transistor is connected with the second clock signal end, a source of the eighth transistor is connected with the high level end, and a drain of the eight transistor is connected with the second control node B.

[0016] the second pull-down unit comprises a ninth transistor and a third capacitor, a gate of the ninth transistor is connected with the second control node B, a source of the ninth transistor is connected with the low level end, a drain of the ninth transistor is connected with the second output end, and two ends of the third capacitor are connected with the source and the drain of the ninth transistor, respectively.

[0017] the second pull-up unit comprises a tenth transistor and a fourth capacitor, a gate of the tenth transistor is connected with the first control node A, a source of the tenth transistor is connected with the high level end, a drain of the tenth transistor is connected with the second output end, and two ends of the fourth capacitor are connected with the drain of the tenth transistor and the drain of the eight transistor, respectively.

[0018] According to another aspect of the embodiments of the present disclosure, there is provided a shift register circuit, comprising a plurality of the above mentioned shift register units connected in series.

[0019] Except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit.

[0020] The shift register circuit comprises a first shift register unit set and a second shift register unit set, each of the shift register unit sets comprises a plurality of the shift register units connected in series.

[0021] In each of the shift register unit sets, except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit.

[0022] Clock signals inputted into the first shift register unit set comprise a first clock signal and a second clock signal.

[0023] Clock signals inputted into the second shift register unit set comprise a third clock signal and a fourth clock signal.

[0024] The first clock signal is a half clock period apart from the third clock signal.

[0025] The second clock signal is a half clock period apart from the fourth clock signal.

[0026] According to another aspect of the embodiments of the present disclosure, there is provided an array substrate on which are formed the above mentioned shift register circuit.

[0027] According to another aspect of the embodiments of the present disclosure, there is provided a display device, comprising:

OLED display means for displaying an image; and

a shift register circuit for driving the OLED display means, and

the shift register circuit is the above mentioned shift register circuit.

[0028] The embodiments of the present disclosure provide a shift register unit, a shift register circuit, an array substrate and a display device, wherein, the shift register unit is used to control a driving TFT for driving an OLED device to coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] In order to describe more clearly technical solutions according to the embodiments of the present disclosure or the prior art, drawings needed in the description of the embodiments or the prior art will be introduced briefly. Obviously, the figures in the following description are merely some embodiments of the present disclosure, and for those of ordinary skill in the art, other figures can further be obtained according to these figures without inventive works.

[0030] FIG. **1** is a structural schematic diagram of a shift register unit according an embodiment of the present disclosure;

[0031] FIG. **2** is a structural schematic diagram of another shift register unit according an embodiment of the present disclosure;

[0032] FIG. **3** is a structural schematic diagram of a circuit connection of a shift register unit according an embodiment of the present disclosure;

[0033] FIG. **4** is a schematic diagram of a clock signal timing state of a shift register unit according an embodiment of the present disclosure;

[0034] FIG. **5** is a structural schematic diagram of a shift register circuit according an embodiment of the present disclosure;

[0035] FIG. **6** is a structural schematic diagram of another shift register circuit according an embodiment of the present disclosure; and

[0036] FIG. **7** is a schematic diagram of a clock signal timing state of another shift register unit according an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0037] The technical solutions in the embodiments of the present disclosure will be described clearly and completely below in conjunction with the drawings in the embodiments of the present disclosure. Obviously, the described embodiments are merely a part of the embodiment instead of all the embodiments. Based on the embodiments of the present disclosure, all other embodiments obtained by those of ordinary skill in the art without inventive works belong to the scope protected by the present disclosure.

[0038] All transistors adopted in all the embodiments of the present disclosure can be thin film transistor, FETs or other devices having identical characteristics. Since the source and

the drain of the transistor adopted here are symmetrical, its source and drain have no difference. In the embodiments of the present disclosure, in order to differentiate the two electrodes except the gate, of the transistor, one of them is called a source and the other one is called a drain. It is prescribed according to the form in the figures that, the central end of the transistor is the gate, the signal input end is the source and the signal output end is the drain. In addition, all the transistors adopted in the embodiments of the present disclosure are P type transistor, that is, they are turned on when the gate is at a low level.

[0039] The structure of a shift register according to the embodiments of the present disclosure is as shown in FIG. **1**, comprising:

A first pull-up unit **1** connected with a high level end VGH, a first clock signal end CLK**1** and a control node A.

A first pull-down unit **2** connected with a low level end VGL, a second clock signal end CLK**2**, an input signal end INPUT, the first pull-up unit **1**, a first output end EM**1** and the control node A.

A pull-down switch unit **3** connected with the high level end VGH, the low level end VGL, the first clock signal end CLK**1**, the second clock signal end CLK**2** and a control node B.

A second pull-down unit **4** connected with the low level end VGL, the control node B and the second output end EM**2**.

A second pull-up unit **5** connected with the high level end VGH, the control node A and the second output end EM**2**.

[0040] Wherein, the first pull-up unit **1** is used to pull up a level of the control node A when a low level is inputted into the first clock signal end CLK**1**; the first pull-down unit **2** is used to pull down the level of the control node A when a low level is inputted into both of the second clock signal end CLK**2** and the input signal end INPUT, respectively; the pull-down switch unit **3** is used to pull down a level of the control node B when a low level is inputted into the first clock signal end CLK**1**, and pull up the level of the control node B when a low level is inputted into the second clock signal end CLK**2**; the second pull-up unit **5** is used to pull up a level outputted from the second output end EM**2** when the control node A is at a low level, to output a driving signal; and the second pull-down unit **4** is used to pull down the level outputted from the second output end EM**2** when the control node B is at a low level, to reset the driving signal.

[0041] The shift register unit according to the embodiments of the present disclosure is used to control a driving TFT for driving an OLED device, coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

[0042] Further, as shown in FIG. **2**, in the shift register according to the embodiments of the present disclosure, the first pull-up unit **1** can further comprise:

A first pull-up module **11** connected with the high level end VGH, the first clock signal end CLK**1** and a control node C.

A second pull-up module **12** connected with the high level end VGH, the first clock signal end CLK**1** and a control node D.

A third pull-up module **13** connected with the high level end VGH, the first clock signal end CLK**1** and the control node A.

[0043] Correspondingly, the first pull-down unit **2** comprises:

A first pull-down module **21** connected with the input signal end INPUT and the control node C.

A second pull-down module **22** connected with the second clock signal end CLK**2**, the control node C and the control node D.

A third pull-down module **23** connected with the low level end VGL, the control node D and the control node A.

[0044] Wherein the first output end EM**1** is connected with the control node D.

[0045] The first pull-up module **11** and the first pull-down module **21** determine the magnitude of the level of the control node C, and thus can control the switch state of the second pull-down module **22**. Further, the second pull-down module **22** and the second pull-up module **12** together determine the level of the control node D, and thus control the switch state of the third pull-down module **23**. The pull-down module **23** and the third pull-up module **13** determine the level of the control node A. The first output end EM**1** is used to provided input signal INPUT to a next level shift register.

[0046] More further, as shown in FIG. **3**, the first pull-up module **11** comprises a first transistor T**1** whose gate is connected with the first clock signal end CLK**1**, whose source is connected with the high level end VGH and whose drain is connected with the control node C.

[0047] The second pull-up module **12** comprises a second transistor T**2** whose gate is connected with the first clock signal end CLK**1**, whose source is connected with the high level end VGH and whose drain is connected with the control node D.

[0048] The third pull-up module **13** comprises a third transistor T**3** whose gate is connected with the first clock signal end CLK**1**, whose source is connected with the high level end VGH and whose drain is connected with the control node A.

[0049] The first pull-down module **21** comprises a fourth transistor T**4** whose gate and source are connected with the input signal end INPUT, and whose drain is connected with the control node C.

[0050] The second pull-down module **22** comprises a fifth transistor T**5** and a first capacitor C**2**, a gate of the fifth transistor T**5** is connected with the control node C, a source of the fifth transistor T**5** is connected with the second clock signal end CLK**2**, a drain of the fifth transistor T**5** is connected with the control node D, and two ends of the first capacitor C**2** are connected with the gate and the source of the fifth transistor T**5**, respectively.

[0051] The third pull-down module **23** comprises a sixth transistor T**6** and a second capacitor C, a gate of the sixth transistor T**6** is connected with the control node D, a source of the sixth transistor T**6** is connected with the low level end VGL, a drain of the sixth transistor T**6** is connected with the control node A, and two ends of the second capacitor C**2** are connected with the source and the drain of the sixth transistor T**6**, respectively. One end of C**2** and the source of T**6** both connect with low level end.

[0052] The pull-down switch unit **3** comprises a seventh transistor T**7** and an eighth transistor T**8**, a gate of the seventh transistor T**7** is connected with the first clock signal end CLK**1**, a source of the seventh transistor T**7** is connected with the low level end VGL, a drain of the seventh transistor T**7** is connected with the control node B, a gate of the eighth tran-

sistor T8 is connected with the second clock signal end CLK2, a source of the eighth transistor T8 is connected with the high level end VGH, and a drain of the eight transistor T8 is connected with the control node B.

[0053] The second pull-down unit **4** comprises a ninth transistor T9 and a third capacitor C3, a gate of the ninth transistor T9 is connected with the control node B, a source of the ninth transistor T9 is connected with the low level end VGL, a drain of the ninth transistor T9 is connected with the second output end EM2, and two ends of the third capacitor C3 are connected with the source and the drain of the ninth transistor T9, respectively.

[0054] The second pull-up unit **5** comprises a tenth transistor T10 and a fourth capacitor C4, a gate of the tenth transistor T10 is connected with the control node A, a source of the tenth transistor T10 is connected with the high level end VGH, a drain of the tenth transistor T10 is connected with the second output end EM2, and two ends of the fourth capacitor C4 are connected with the drain of the tenth transistor T10 and the drain of the eight transistor T8, respectively.

[0055] The shift register unit according to the embodiments of the present disclosure is used to control a driving TFT for driving an OLED device to coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

[0056] The work state of the shift register unit according to the embodiments of the present disclosure as shown in FIG. **3** will be described in detail below in conjunction with the timing state diagram shown in FIG. **4**.

[0057] t1 state: the first clock signal CLK1 is at a high level, and both the signal INPUT (herein, a frame start signal STV is taken as an example of the input signal) and the second clock signal CLK2 are at a low level. At this time, the transistor T4 is turned on, the control node C is pull down, and the transistor T5 is turned on. In the meantime, since the first clock signal CLK1 is at a high level, all of the transistor T1, T2 and T3 are turned off. Therefore, since the transistor T6 is turned on, the second clock signal CLK2 is at a low level, the level of the control node D is at a low level and the first output end EM1 is at a low level at this time. In the meantime, since the transistor T6 is turned on, the level of the control node A is at a low level VGL, then the transistor T10 is turned on, and the second output end EM2 is correspondingly at a high level VGH. In the meantime, since the first clock signal CLK1 is at a high level, the transistors T7 and T9 are turned off, thus ensuring the input of the second output end EM2 is not affected by the transistors T7 and T9. At this time, the second output end EM2 is at a high level, so as to complete the input of the driving current of the OLED device.

[0058] t2 stage: both the signal INPUT and the second clock signal CLK2 are at a high level, and the first clock signal CLK1 is at a low level. At this time, the transistor T4 is turned off. In the meantime, since the first clock signal CLK1 is at a low level, the transistors T1, T2 and T3 are all turned on, then the level of the control node D is pulled up to a high level, thus causing that the transistor T6 turned off and the first output end EM1 is at a high level. Since the transistor T3 is turned on, the level of the control node A is at a high level and the transistor T10 is turned off. In the meantime, since the first clock signal CLK1 is at a low level and the second clock signal CLK2 is at a high level at this time, the transistor T7 is turned on, T8 is turned off, the level of the control node B is at a low level, and thus the transistor T9 is turned on. At this time, the output of the second output end EM2 is at a low level, completing resetting of the input.

[0059] The embodiments of the present disclosure can be achieved by N type transistors by adjusting the timings of the input signals.

[0060] As shown in FIG. **5**, the shift register circuit according to the embodiments of the present disclosure comprises a plurality of the shift register units connected in series.

[0061] Except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit.

[0062] Specifically, the shift register circuit as shown in FIG. **5** comprises several shift register units connected in series, in which, a first output end EM1_1 of a shift register unit S1 is connected with an input end INPUT2 of a shift register unit S2, its second output end EM2_1 is connected with a gate of a driving TFT, and the driving TFT is used for accurately controlling a driving current of a row of OLED devices; a first output end EM1_2 of a shift register unit S2 is connected with an input end INPUT3 of a shift register unit S3, its second output end EM2_2 is connected with a gate of another driving TFT, and this driving TFT is used for accurately controlling a driving current of another row of OLED devices; the other shift register units are connected according this method, and each shift register unit has a first clock signal end CLK1 and a second clock signal end CLK2, wherein, the first clock signal CLK1 is connected with a system clock signal CLOCLK1, and a second clock signal CLK2 is connected with a system clock signal CLOCLK2. Wherein the duty cycles of low levels of the system clock signals CLOCLK1 and CLOCLK2 are both 1:2, and the low level signal of CLOCLK2 begins after the end of the low level signal of CLOCLK1, the next low level signal of CLOCLK1 begins after the end of the low level signal of CLOCLK2, and such a cycle continues thereafter. In the present embodiment, the first shift register unit is the shift register unit S1, then the input signal INPUT1 of the shift register unit S1 is an active pulse signal, such as optionally the frame start signal STV, at this time, the low level signal of the STV and the system clock signal CLOCLK1 begin simultaneously, and end simultaneously.

[0063] Wherein, the shift register unit according to the embodiments of the present disclosure is used to control a driving TFT for driving an OLED device to coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

[0064] Further, as shown in FIG. **6**, the shift register circuit comprises a first shift register unit set and a second shift register unit set, each of the shift register unit sets comprises a plurality of the shift register units connected in series.

[0065] In each of the shift register unit sets, except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit.

[0066] Specifically, in the shift register circuit as shown in FIG. **6**, the shift register units S**1**, S**3**, S**5** . . . are the first shift register unit set, and shift register units S**2**, S**4**, S**6**, . . . are the second shift register set. Refer to FIG. **5** for the connection of each of the shift register unit sets.

[0067] Wherein, clock signals inputted into the first shift register unit set comprise a first clock signal and a second clock signal.

[0068] Clock signals inputted into the second shift register unit set comprise a third clock signal and a fourth clock signal.

[0069] Specifically, the timing state of the shift register circuit according to the embodiments of the present disclosure can be as shown in FIG. **7**. Wherein, the first clock signal CLK**1** is a half clock period apart from the third clock signal CLK**3**, the second clock signal CLK**2** is a half clock period apart from the fourth clock signal CLK**4**. A control signal using such a timing can effectively separate out a time slot between each level of shift register circuits, thus avoiding interferences of current between the shift register circuits.

[0070] In addition, the embodiments of the present disclosure provides an array substrate, on which are formed a shift register circuits, and the shift register circuit is the above mentioned shift register circuit.

[0071] By using such an array substrate, the shift register unit is used to control a driving TFT for driving an OLED device to coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

[0072] The embodiment of the present disclosure further provides a display device, such as a display panel, comprising:

OLED display means for displaying an image.

A shift register circuit for driving the OLED display means.

[0073] The shift register circuit is the above mentioned shift register circuit.

[0074] A display device provided by the embodiment of the present disclosure includes a shift register circuit. Wherein, the shift register unit is used to control a driving TFT for driving an OLED device to coordinate with an existing shift register unit for controlling a pixel circuit, control the driving TFT to turn off the driving current of the OLED device when the shift register unit for controlling the pixel circuit writes data into the pixel circuit, and control the driving TFT again to turn on the OLED device when the writing of the data is finished. As such, a problem of flickers can be prevented from occurring in the OLED display device while writing display data, and the product quality of the OLED display device is enhanced.

[0075] What is described is merely the specific mode for implementing the present disclosure, but the protection scope of the present disclosure is not limited thereto. Variations or alternations occurred to any skilled in the art within the technical scope disclosed by the present disclosure should be covered by the protection scope of the present disclosure. Therefore, the protection scope of the present disclosure is subject to the protection scope of the claims.

1. A shift register unit comprising:

a first pull-up unit connected with a high level end, a first clock signal end and a first control node (A);

a first pull-down unit connected with a low level end, a second clock signal end, an input signal end, the first pull-up unit, a first output end and the first control node (A);

a pull-down switch unit connected with the high level end, the low level end, the first clock signal end, the second clock signal end and a second control node (B);

a second pull-down unit connected with the low level end, the second control node (B) and a second output end; and

a second pull-up unit connected with the high level end, the first control node (A) and the second output end;

wherein, the first pull-up unit is used to pull up a level of the first control node (A) when a low level is inputted into the first clock signal end; the first pull-down unit is used to pull down the level of the first control node (A) when a low level is inputted into both of the second clock signal end and the input signal end; the pull-down switch unit is used to pull down a level of the second control node (B) when a low level is inputted into the first clock signal end, and pull up the level of the second control node (B) when a low level is inputted into the second clock signal end; the second pull-up unit is used to pull up a level outputted from the second output end when the first control node (A) is at a low level, to output a driving signal; and the second pull-down unit is used to pull down the level outputted from the second output end when the second control node (B) is at a low level, to reset the driving signal.

2. The shift register unit according to claim **1**, wherein

the first pull-up unit comprises:

a first pull-up module connected with the high level end, the first clock signal end and a third control node (C);

a second pull-up module connected with the high level end, the first clock signal end and a fourth control node (D); and

a third pull-up module connected with the high level end, the first clock signal end and the first control node (A),

the first pull-down unit comprises:

a first pull-down module connected with the input signal end and the third control node (C);

a second pull-down module connected with the second clock signal end, the third control node (C) and the fourth control node (D); and

a third pull-down module connected with the low level end, the fourth control node (D) and the first control node (A), and

wherein the first output end is connected with the fourth control node (D).

3. The shift register unit according to claim **2**, wherein

the first pull-up module comprises a first transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the third control node (C);

the second pull-up module comprises a second transistor having a gate connected with the first clock signal end,

having a source connected with the high level end and having a drain connected with the fourth control node (D);

the third pull-up module comprises a third transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the first control node (A);

the first pull-down module comprises a fourth transistor having a gate and source connected with the input signal end, and having a drain connected with the third control node (C);

the second pull-down module comprises a fifth transistor and a first capacitor, a gate of the fifth transistor is connected with the third control node (C), a source of the fifth transistor is connected with the second clock signal end, a drain of the fifth transistor is connected with the fourth control node (D), and two ends of the first capacitor are connected with the gate and the source of the fifth transistor, respectively;

the third pull-down module comprises a sixth transistor and a second capacitor, a gate of the sixth transistor is connected with the fourth control node (D), a source of the sixth transistor is connected with the low level end, a drain of the sixth transistor is connected with the first control node (A), and two ends of the second capacitor are connected with the source and the drain of the sixth transistor, respectively;

the pull-down switch unit comprises a seventh transistor and an eighth transistor, a gate of the seventh transistor is connected with the first clock signal end, a source of the seventh transistor is connected with the low level end, a drain of the seventh transistor is connected with the second control node (B), a gate of the eighth transistor is connected with the second clock signal end, a source of the eighth transistor is connected with the high level end, and a drain of the eight transistor is connected with the second control node (B);

the second pull-down unit comprises a ninth transistor and a third capacitor, a gate of the ninth transistor is connected with the second control node (B), a source of the ninth transistor is connected with the low level end, a drain of the ninth transistor is connected with the second output end, and two ends of the third capacitor are connected with the source and the drain of the ninth transistor, respectively; and

the second pull-up unit comprises a tenth transistor and a fourth capacitor, a gate of the tenth transistor is connected with the first control node (A), a source of the tenth transistor is connected with the high level end, a drain of the tenth transistor is connected with the second output end, and two ends of the fourth capacitor are connected with the drain of the tenth transistor and the drain of the eight transistor, respectively.

4. A shift register circuit comprising a plurality of the shift register units of claim **1**, connected in series,

except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit.

5. The shift register circuit according to claim **4**, wherein the shift register circuit comprises a first shift register unit set and a second shift register set, each of the shift register unit sets comprises a plurality of the shift register units connected in series,

in each of the shift register unit sets, except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit;

clock signals inputted into the first shift register unit set comprise a first clock signal and a second clock signal; and

clock signals inputted into the second shift register unit set comprise a third clock signal and a fourth clock signal.

6. The shift register circuit according to claim **5**, wherein

the first clock signal is a half clock period apart from the third clock signal; and

the second clock signal is a half clock period apart from the fourth clock signal.

7. (canceled)

8. A display device, comprising:

OLED display means for displaying an image; and

a shift register circuit for driving the OLED display means,

wherein, the shift register circuit is the shift register circuit according to claim **4**.

9. The shift register circuit according to claim **6**, wherein

the first pull-up unit comprises:

a first pull-up module connected with the high level end, the first clock signal end and a third control node (C);

a second pull-up module connected with the high level end, the first clock signal end and a fourth control node (D); and

a third pull-up module connected with the high level end, the first clock signal end and the first control node (A),

the first pull-down unit comprises:

a first pull-down module connected with the input signal end and the third control node (C);

a second pull-down module connected with the second clock signal end, the third control node (C) and the fourth control node (D); and

a third pull-down module connected with the low level end, the fourth control node (D) and the first control node (A), and

wherein the first output end is connected with the fourth control node (D).

10. The shift register circuit according to claim **9**, wherein

the first pull-up module comprises a first transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the third control node (C);

the second pull-up module comprises a second transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the fourth control node (D);

the third pull-up module comprises a third transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the first control node (A);

the first pull-down module comprises a fourth transistor having a gate and source connected with the input signal end, and having a drain connected with the third control node (C);

the second pull-down module comprises a fifth transistor and a first capacitor, a gate of the fifth transistor is connected with the third control node (C), a source of the fifth transistor is connected with the second clock signal end, a drain of the fifth transistor is connected with the

fourth control node (D), and two ends of the first capacitor are connected with the gate and the source of the fifth transistor, respectively;

the third pull-down module comprises a sixth transistor and a second capacitor, a gate of the sixth transistor is connected with the fourth control node (D), a source of the sixth transistor is connected with the low level end, a drain of the sixth transistor is connected with the first control node (A), and two ends of the second capacitor are connected with the source and the drain of the sixth transistor, respectively;

the pull-down switch unit comprises a seventh transistor and an eighth transistor, a gate of the seventh transistor is connected with the first clock signal end, a source of the seventh transistor is connected with the low level end, a drain of the seventh transistor is connected with the second control node (B), a gate of the eighth transistor is connected with the second clock signal end, a source of the eighth transistor is connected with the high level end, and a drain of the eight transistor is connected with the second control node (B);

the second pull-down unit comprises a ninth transistor and a third capacitor, a gate of the ninth transistor is connected with the second control node (B), a source of the ninth transistor is connected with the low level end, a drain of the ninth transistor is connected with the second output end, and two ends of the third capacitor are connected with the source and the drain of the ninth transistor, respectively; and

the second pull-up unit comprises a tenth transistor and a fourth capacitor, a gate of the tenth transistor is connected with the first control node (A), a source of the tenth transistor is connected with the high level end, a drain of the tenth transistor is connected with the second output end, and two ends of the fourth capacitor are connected with the drain of the tenth transistor and the drain of the eight transistor, respectively.

11. The display device according to claim **8**, wherein the shift register circuit comprises a first shift register unit set and a second shift register set, each of the shift register unit sets comprises a plurality of the shift register units connected in series,

in each of the shift register unit sets, except a first shift register unit, an input signal of each of the other shift register units comes from a signal outputted from a first output end of an adjacent shift register unit before the shift register unit;

clock signals inputted into the first shift register unit set comprise a first clock signal and a second clock signal; and

clock signals inputted into the second shift register unit set comprise a third clock signal and a fourth clock signal.

12. The display device according to claim **11**, wherein

the first clock signal is a half clock period apart from the third clock signal; and

the second clock signal is a half clock period apart from the fourth clock signal.

13. The display device according to claim **12**, wherein

the first pull-up unit comprises:

a first pull-up module connected with the high level end, the first clock signal end and a third control node (C);

a second pull-up module connected with the high level end, the first clock signal end and a fourth control node (D); and

a third pull-up module connected with the high level end, the first clock signal end and the first control node (A),

the first pull-down unit comprises:

a first pull-down module connected with the input signal end and the third control node (C);

a second pull-down module connected with the second clock signal end, the third control node (C) and the fourth control node (D); and

a third pull-down module connected with the low level end, the fourth control node (D) and the first control node (A), and

wherein the first output end is connected with the fourth control node (D).

14. The display device according to claim **13**, wherein

the first pull-up module comprises a first transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the third control node (C);

the second pull-up module comprises a second transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the fourth control node (D);

the third pull-up module comprises a third transistor having a gate connected with the first clock signal end, having a source connected with the high level end and having a drain connected with the first control node (A);

the first pull-down module comprises a fourth transistor having a gate and source connected with the input signal end, and having a drain connected with the third control node (C);

the second pull-down module comprises a fifth transistor and a first capacitor, a gate of the fifth transistor is connected with the third control node (C), a source of the fifth transistor is connected with the second clock signal end, a drain of the fifth transistor is connected with the fourth control node (D), and two ends of the first capacitor are connected with the gate and the source of the fifth transistor, respectively;

the third pull-down module comprises a sixth transistor and a second capacitor, a gate of the sixth transistor is connected with the fourth control node (D), a source of the sixth transistor is connected with the low level end, a drain of the sixth transistor is connected with the first control node (A), and two ends of the second capacitor are connected with the source and the drain of the sixth transistor, respectively;

the pull-down switch unit comprises a seventh transistor and an eighth transistor, a gate of the seventh transistor is connected with the first clock signal end, a source of the seventh transistor is connected with the low level end, a drain of the seventh transistor is connected with the second control node (B), a gate of the eighth transistor is connected with the second clock signal end, a source of the eighth transistor is connected with the high level end, and a drain of the eight transistor is connected with the second control node (B);

the second pull-down unit comprises a ninth transistor and a third capacitor, a gate of the ninth transistor is connected with the second control node (B), a source of the ninth transistor is connected with the low level end, a drain of the ninth transistor is connected with the second

output end, and two ends of the third capacitor are connected with the source and the drain of the ninth transistor, respectively; and

the second pull-up unit comprises a tenth transistor and a fourth capacitor, a gate of the tenth transistor is connected with the first control node (A), a source of the tenth transistor is connected with the high level end, a drain of the tenth transistor is connected with the second output end, and two ends of the fourth capacitor are connected with the drain of the tenth transistor and the drain of the eight transistor, respectively.

* * * * *

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摘要(译)

提供移位寄存器单元，移位寄存器电路，阵列基板和显示装置。本公开涉及显示装置制造领域，并且可以在写入显示数据时防止OLED装置闪烁。移位寄存器包括第一上拉单元，与高电平端连接，第一时钟信号端和第一控制节点（A）;第一下拉单元，与低电平端，第二时钟信号端，输入信号端，第一上拉单元，第一输出端和第一控制节点（A）连接;下拉开关单元，与高电平端，低电平端，第一时钟信号端，第二时钟信号端和第二控制节点（B）连接;第二下拉单元，与低电平端，第二控制节点（B）和第二输出端连接;第二上拉单元，与高电平端，第一控制节点（A）和第二输出端连接。